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(54) Abstract Title
Clock frequency difference reduction

(57) Two consecutive correlations are performed on a synchronisation signal, and the frequency of the local oscillator adjusted until the sign of the phase difference changes. A UMTS cellular telephone system 1 comprises a base station 3 which is able to communicate with one or more mobile telephones within a cell 5. In the telephone 7, a receiver/transmitter module 9 is connected to a radio frequency (r.f.) antenna 11 and is modulated by a local oscillator 13. The local oscillator 13 is controlled by a microprocessor 15 which controls the frequency of the local oscillator and receives signals sent from the base station 3 by means of the receiver/transmitter module 9. In order to establish a data link between the base station 3 and the telephone 7, it is necessary to establish synchronisation between the clock in the base station and the local oscillator 13 of the telephone. This is performed using an algorithm which obtains estimates of the sign of the phase error determined by correlating part of a data burst 19 on the PSCH channel 17. On the basis of the sign of the phase error, the frequency of the local oscillator 13 is iteratively modified to improve the frequency error.

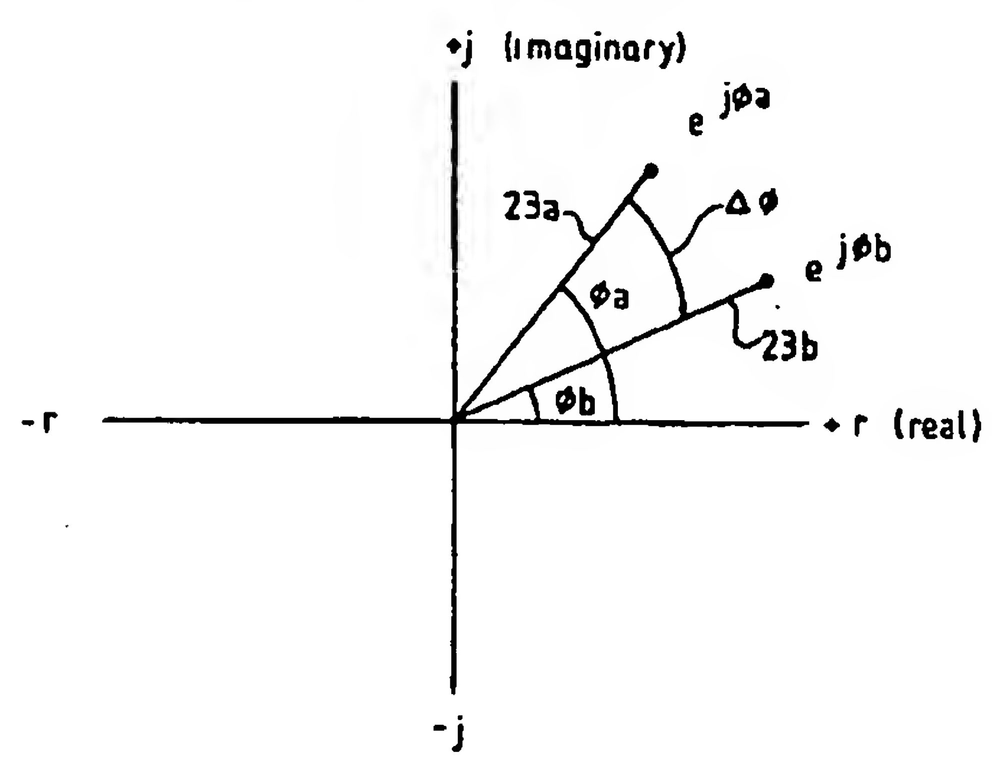

Fig.4.

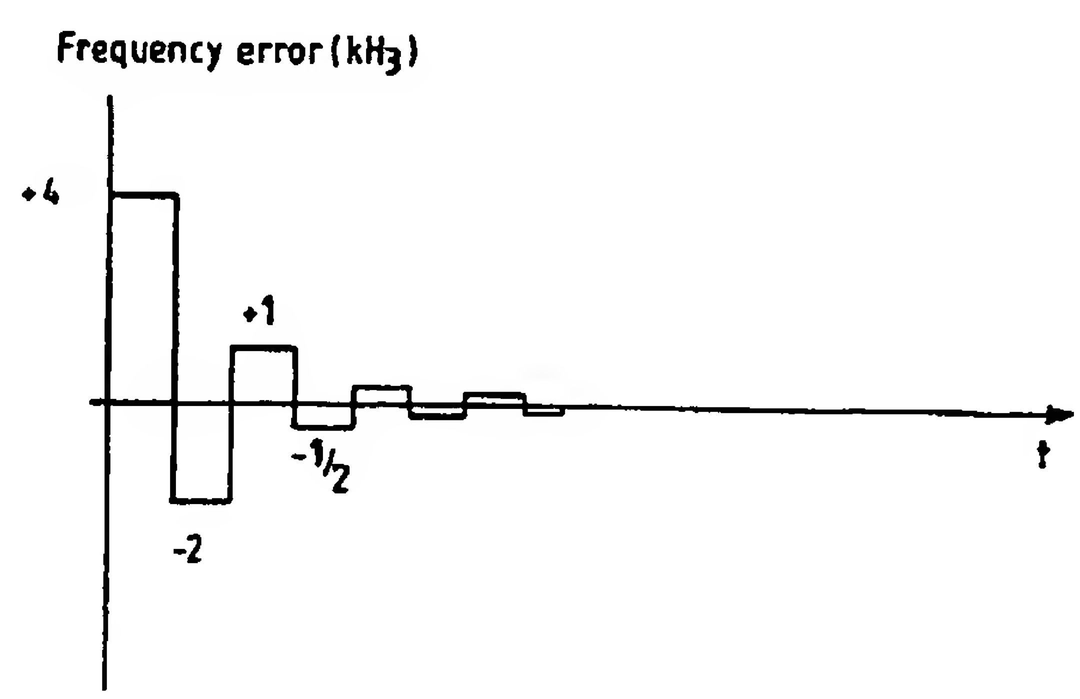

Fig.6.

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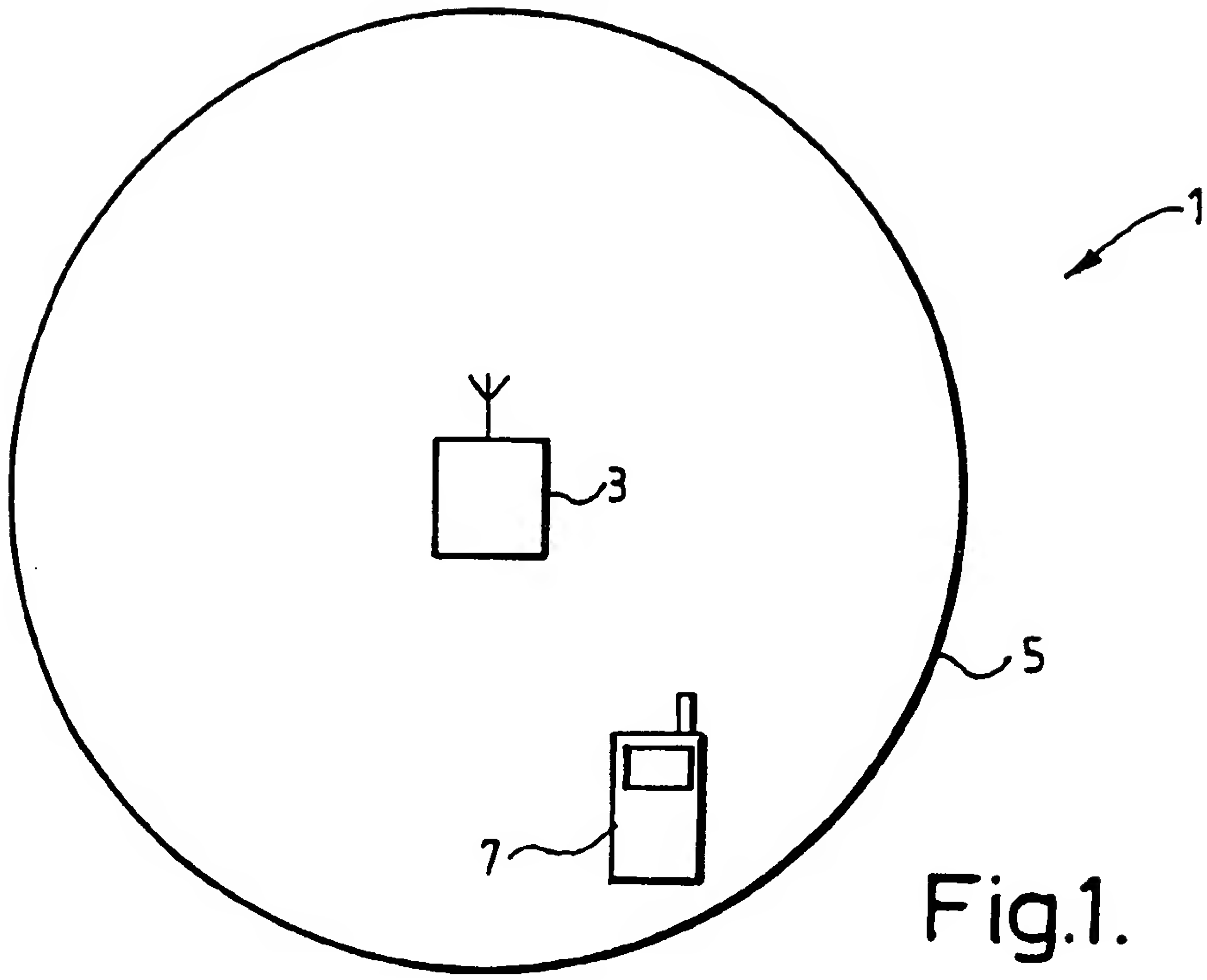

Fig.1.

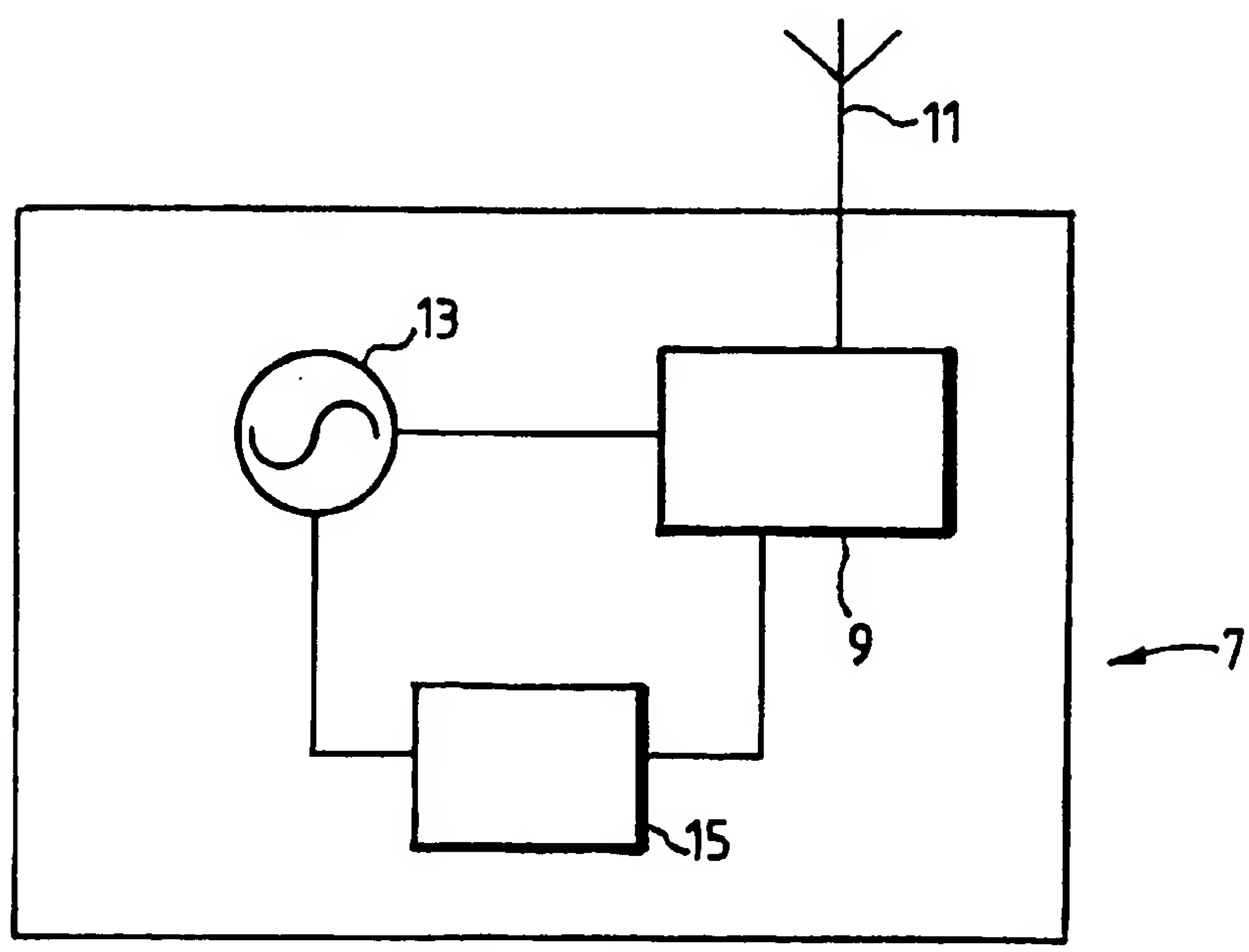

Fig.2.

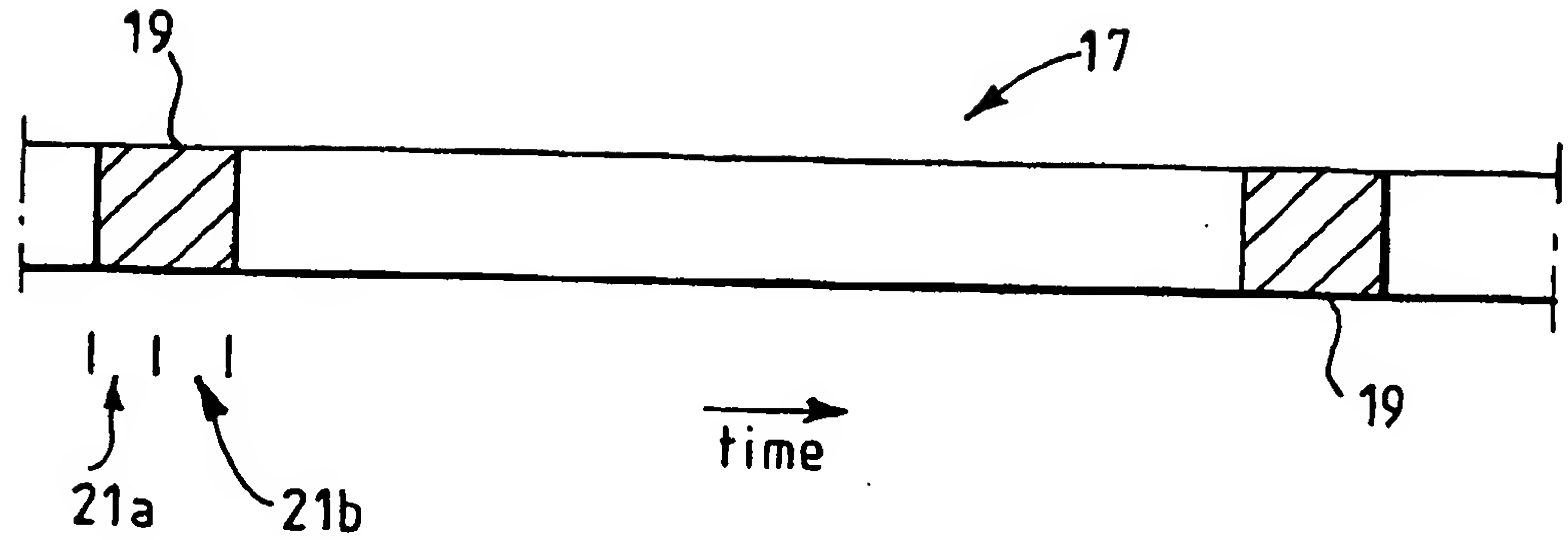
19
17
19
21a
21b
time

Fig.3.

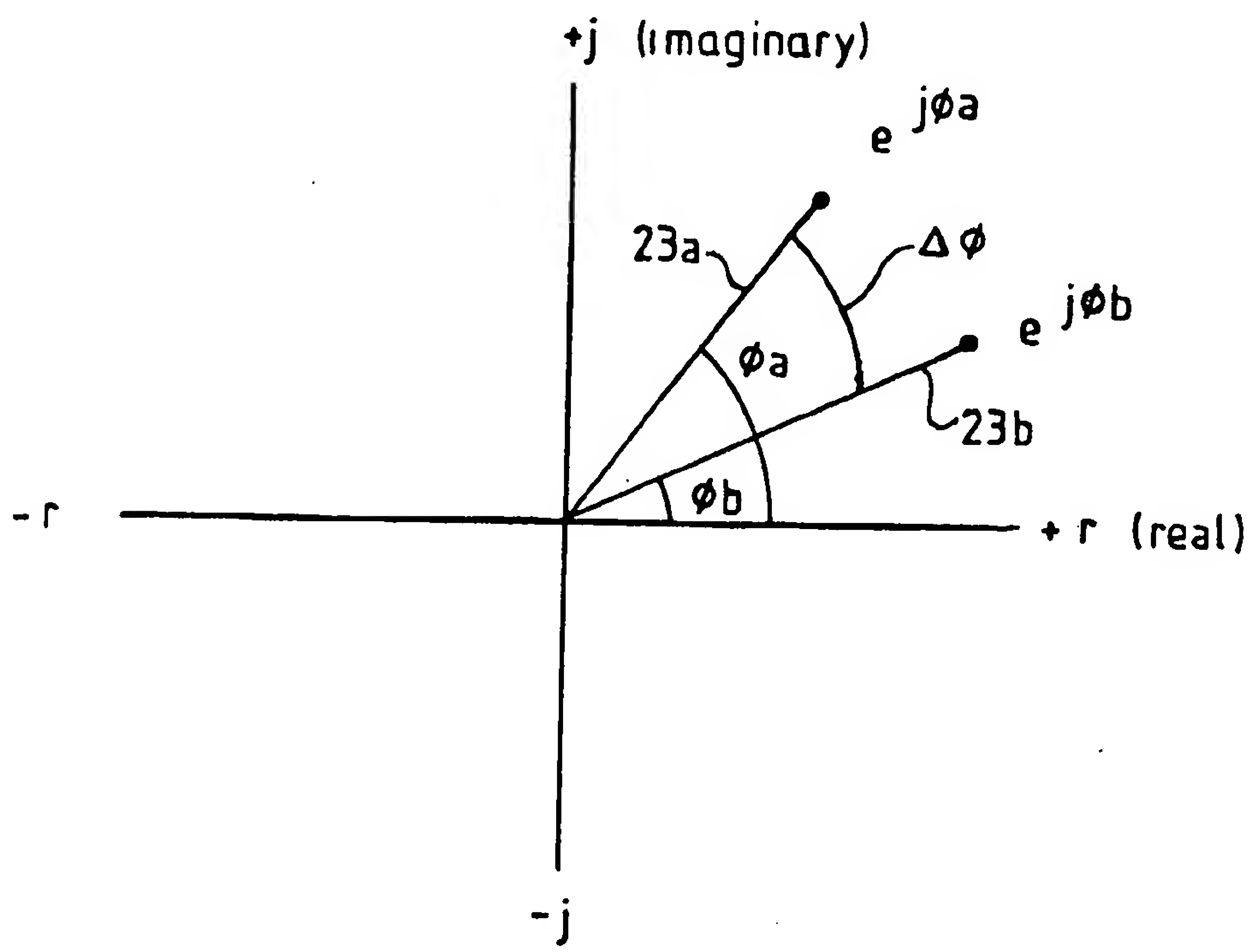
+j (imaginary)
e jøa
23a
Δø
e jøb
øa
23b
øb
-r
+r (real)
-j

Fig.4.

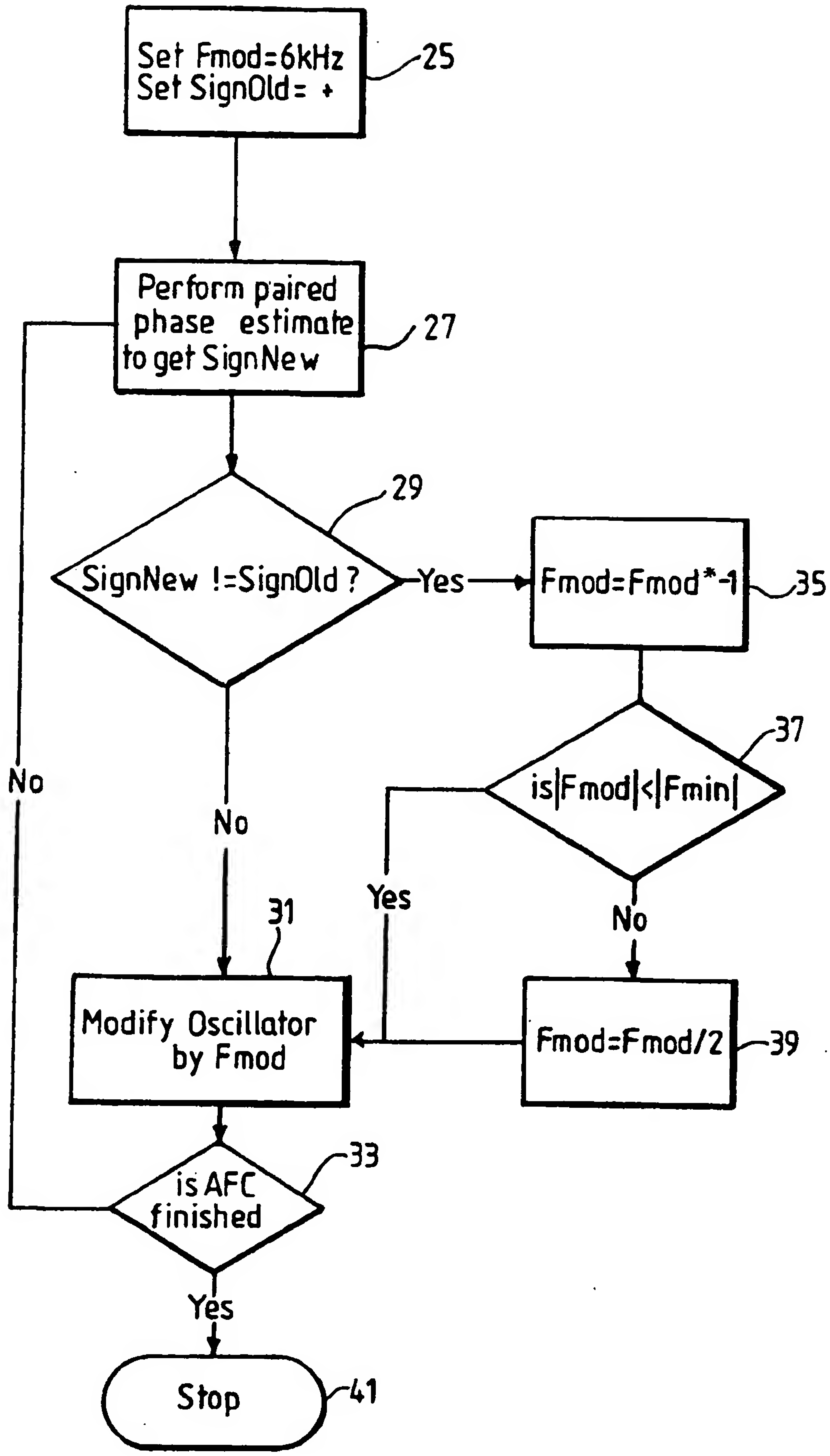
Set Fmod=6kHz
Set SignOld= +
25
Perform paired phase estimate to get SignNew
27
29
SignNew !=SignOld ?
Yes
Fmod=Fmod*-1
35
37
is|Fmod|<|Fmin|
No
No
Yes
No
31
Modify Oscillator by Fmod
Fmod=Fmod/2
39
33
is AFC finished
Yes
Stop
41

Fig.5.

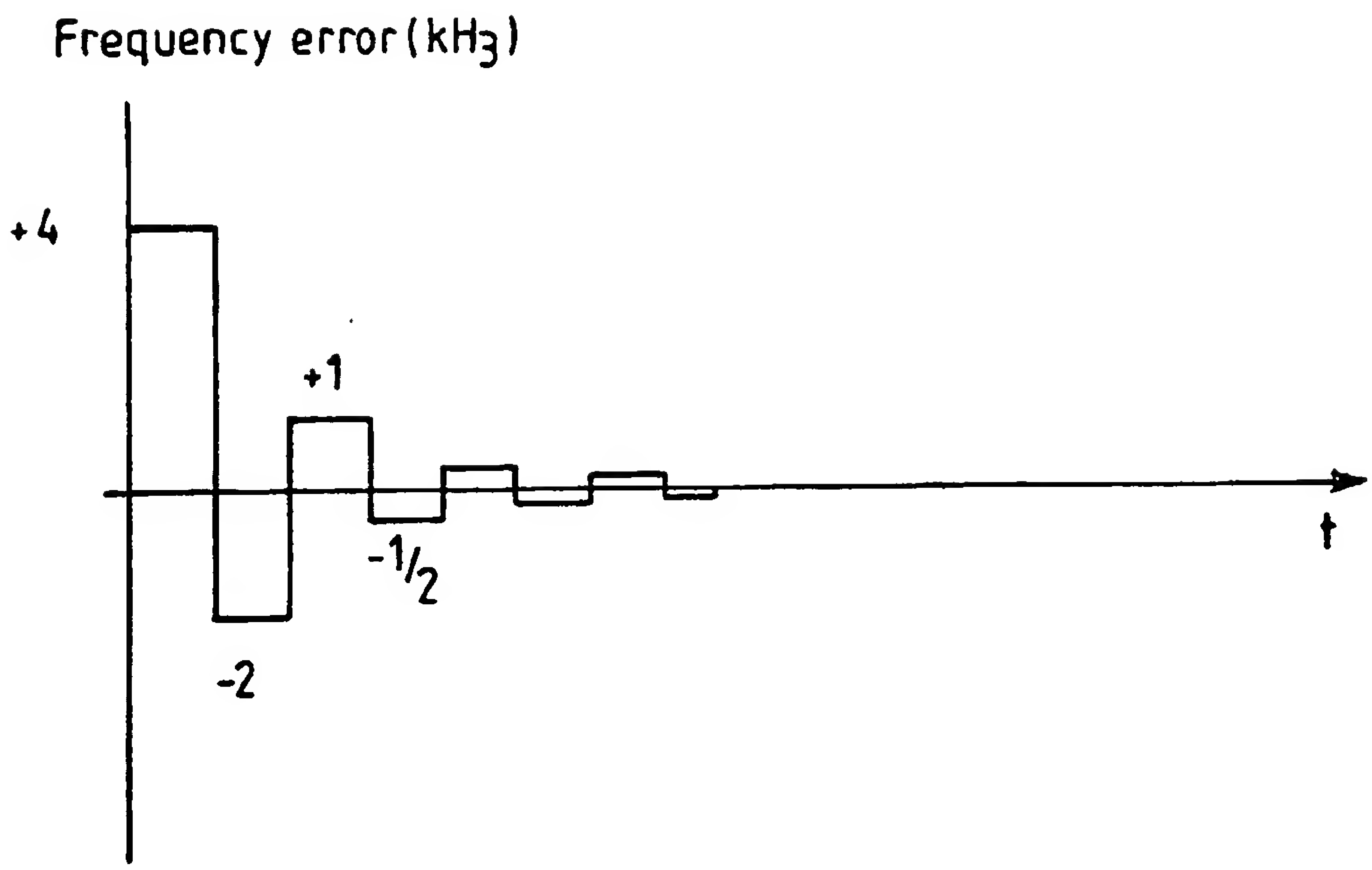

Fig.6.

Frequency Difference Reduction

The invention relates to a method of reducing the frequency difference between a local oscillator of a mobile communications receiver and a clock of a remote base station.

Mobile communications equipment, such as mobile telephones, are now widespread in use. Generally, in order to establish a communications path between the user equipment (UE), e.g. the mobile telephone, and a base station it is necessary to provide synchronisation between a local oscillator of the UE and a clock of the base station. When the UE is turned-on, part of the initial synchronisation procedure is to correct for the frequency difference between the local oscillator in the UE and the local oscillator in the base station. The local oscillator in the UE, which has to be relatively inexpensive for obvious commercial reasons, will exhibit less accuracy than the more expensive and accurate clock in the base station. Accordingly, there is a frequency difference (sometimes called a "frequency error") which has to be corrected.

One form of system which requires such a frequency difference correction is the proposed universal mobile telephone system (UMTS). This system will use code division multiple access (CDMA) to communicate on both uplink and downlink communications channels between base stations and UEs. In this system, it is proposed that so-called automatic frequency control (AFC) is used to provide a coarse estimate of the frequency difference between the local oscillator of a UE and the clock of a base station during the so-called acquisition phase of the UE's operation, i.e. when the UE is initially switched-on. For a crystal with an error specification of 3 parts-per-million, the actual frequency error can be as high as +/- 6 kHz. The estimated frequency difference can then be used to correct the local oscillator.

The current proposal for AFC is to use the timing information provided in the primary synchronisation channel (PSCH) transmitted by the base station. The PSCH has to be used since knowledge of a scrambling code is required to demodulate other code-multiplexed channels. The base station transmits a repeating sequence of 256

chips over the PSCH, each sequence occurring for one tenth of the period of a so-called slot (each slot being 2560 chips in length). An estimate of the frequency difference is made by looking at the phase difference between two consecutive correlations of the repeating sequence and the local oscillator signal (a paired phase-estimate). To avoid potential aliasing, the correlation length used to obtain each phase estimate is 128 chips, and so two correlations of 128 chips are performed on consecutive halves of the 256 chip PSCH sequence. From the phase difference can be calculated the frequency difference, the frequency of the UE's local oscillator thereafter being modified to account for the calculated frequency difference. This is explained mathematically by:

phase difference = $\Delta\varnothing$

frequency difference = Δf

phase difference in terms of frequency difference : $\Delta\varnothing = (2\pi\Delta f t) \bmod 2\pi$

(where t is the length of the correlation in seconds)

so, $\Delta f = \Delta\varnothing / 2\pi t$

Where there is little or no noise, i.e. a high signal-to-noise ratio (SNR), this conventional method will work sufficiently well. When there is noise present, as is usually the case (reasonably up to 5 dB being present), the estimate of the phase difference may be very poor, and so the estimated frequency difference is similarly poor. This is not helped by the fact that the power level of the PSCH is very low (-15 dB). This can be partly compensated for by averaging the estimates of the phase difference and applying low pass filtering. However, a problem which arises from this filtering is that the convergence of the UE's local oscillator with the base station clock takes much longer. This prolonged period during which there is a frequency difference can cause a timing drift between the UE local oscillator and the base station. If this timing drift becomes large (greater than about half a chip) then the correlation on the PSCH will fail and synchronisation is lost. The position of the PSCH must be re-obtained. The need for re-synchronisation should be avoided.

Once the frequency difference is reduced using the AFC technique on the PSCH, the scrambling code can be more reliably obtained from a so-called Common Pilot Channel (CPICH) without the worry of frequency aliasing. The CPICH, which is transmitted at a higher power that the PSCH can be used to reduce further, with higher accuracy, the frequency difference (reducing the frequency difference to almost zero). The method described herein relates to the more 'coarse' method which enables some initial degree of synchronisation to be achieved.

According to a first aspect of the present invention, there is provided a method of reducing the frequency difference between a local oscillator of a mobile communications receiver and a clock of a remote base station, the method comprising: receiving, at the mobile communications receiver, a synchronisation signal representative of the clock of the base station; performing two consecutive correlation operations on the synchronisation signal to generate an estimate of the sign of the phase difference between the local oscillator and the synchronisation signal; and modifying the local oscillator frequency until the sign of the phase difference changes.

The method provides a means by which an initial adjustment of frequency difference is made, without analysing the magnitude of the phase estimate (as relied upon by conventional methods). In the method, only an estimate of the sign of the phase difference is used. On this basis, the local oscillator frequency is modified until the sign of the phase difference changes, which can be, for example, from positive to zero, from positive to negative, from negative to zero, or from negative to positive. Once the sign changes, this provides an indication that the zero error mark has been reached, or crossed, and so a reduced phase difference, and so frequency difference, can be attained. The magnitude of the phase difference, which is liable to interference from noise, is not relied upon and no low pass filtering is required.

In the case of UMTS, by reducing the frequency difference, it increases the probability of being able to descramble and demodulate other physical channels which are transmitted at a higher power and so can be used to generate a 'finer' estimate of the difference and so may provide a more accurate synchronisation.

The step of modifying the local oscillator frequency preferably comprises modifying the frequency by one or more steps of a predetermined amount.

After the sign of the phase difference changes, the method may further comprise: modifying the local oscillator frequency by one or more steps of a further predetermined amount until the estimated sign of the phase difference changes again, the further predetermined amount being less than that of the previous predetermined amount. The local oscillator frequency may be repeatedly modified until the further predetermined amount is reduced to reach a minimum predefined level which is indicative of the phase difference converging around a zero error mark.

In this way, the method used can be considered a 'successive approximation' method whereby the local oscillator frequency changes in steps of reducing magnitude such that the estimated phase difference converges around the zero error mark. The further predetermined amount may be made equal to approximately one half of the previous predetermined amount.

In between each modification step, a further two correlation operations (a paired phase estimate) are preferably performed to provide an updated estimate of the sign of the phase difference. Thus, after a first correlation operation is performed to generate an estimate of the sign of the phase difference, and the local oscillator frequency modified, another correlation operation is then performed prior to the next modification taking place.

The mobile communications receiver may be configured to receive the synchronisation signal over a spread spectrum communications channel. The spread spectrum communications channel may transmit data using CDMA modulation. The mobile communications receiver may be configured for use with UMTS, the synchronisation signal being received by means of the PSCH. The method may further comprise: after synchronisation is achieved using the PSCH channel, demodulating a further communications channel to provide a further source of synchronisation. As mentioned

above, this may be a channel having greater power than the PSCH channel making it possible to achieve a more accurate estimate of phase difference. In effect, the initial method (using the PSCH channel) becomes a coarse AFC method, with the new channel providing a 'finer' AFC.

In accordance with a second aspect of the invention, there is provided a mobile communications receiver for receiving data from a remote base station, the communications receiver comprising: a local oscillator; and a local oscillator controller, the local oscillator controller being arranged to receive a synchronisation signal representative of the clock of the remote base station, to perform two consecutive correlation operations on the synchronisation signal to generate an estimate of the sign of the phase difference between the local oscillator and the synchronisation signal, and to modify the local oscillator frequency until the sign of the phase difference changes.

Preferred aspects relating to such a mobile communications receiver are defined in the appended set of claims.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a representation of a UMTS cellular telephone system;

Figure 2 is a block diagram showing the elements of a mobile telephone for use in the UMTS system of Figure 1;

Figure 3 illustrates a PSCH channel used as part of the UMTS system of Figure 1;

Figure 4 is a phasor diagram showing the phase difference between two correlation operations made using the PSCH channel shown in Figure 3;

Figure 5 is a flow diagram representing an algorithm for performing frequency adjustment of a local oscillator forming part of the mobile telephone shown in Figure 2; and

Figure 6 is a graph illustrating the effect of performing the algorithm represented in Figure 5.

Referring to Figure 1, a UMTS cellular telephone system 1 comprises a base station 3 which is able to communicate with one or more mobile telephones within a cell, represented here by reference numeral 5. A single telephone 7 is shown within the cell 5.

Figure 2 shows the basic elements within the telephone 7. A receiver/transmitter module 9 is connected to a radio frequency (r.f.) antenna 11. The receiver/transmitter module 9 is modulated by a local oscillator 13 which is a crystal having an error specification of 3 parts-per-million. The local oscillator 13 is controlled by a microprocessor 15. The microprocessor 15 itself receives signals sent from the base station 3 by means of the receiver/transmitter module 9.

The base station 3 includes a very accurate clock (not shown). In order to establish a data link between the base station 3 and the telephone 7, it is necessary to establish synchronisation between the clock in the base station and the local oscillator 13 of the telephone. In this respect it will be appreciated that the local oscillator 13 will be of a lower accuracy than the clock in the base station 3. This is due to cost considerations, bearing in mind the need to keep the cost of the telephone 7 to a reasonable level. Indeed, at 2 Ghz, a frequency difference of +/- 6 kHz can occur. In this UMTS cellular telephone system 1, the so-called PSCH channel is used to assist in reducing the frequency difference to such an extent that synchronisation can be achieved. The existence of the PSCH channel in UMTS will be well known to those skilled in the art.

Figure 3 shows a representation of a PSCH channel 17 established between the base station 3 and the telephone 7. Unlike other UMTS channels, the PSCH channel 17 is

located as part of the synchronisation process. This initial stage is often referred to as the "acquisition" stage. As Figure 3 shows, the PSCH channel includes a repeating burst of data (shown in black and represented by reference numeral 19). Each burst last 256 chips and forms one-tenth of each PSCH frame (of length 2560 chips).

After powering up the telephone 7, the microprocessor 9 receives data transmitted over the PSCH channel 17, by means of the receiver/transmitter module 9, in its acquisition stage. The microprocessor 9 then obtains an estimate of the sign of the phase difference between the base station clock (represented in the burst 19) and the signal currently being generated by the local oscillator 13. It will be noted that 'phase difference' is referred to above. It will be appreciated that it is straightforward to convert from the phase difference to the frequency difference (a complete explanation of the mathematics involved being given above). The term phase difference is used here for ease of explanation, particularly with regard to the phasor diagram of Figure 4, but it should be remembered that the terms "phase difference" and "frequency difference" may be interchanged.

The microprocessor 9 obtains an estimate of the sign of the phase difference by means of performing two consecutive correlations. The first correlation uses the first 128 chips 21a of the burst 19, and the second correlation uses the second 128 chips 21b of the burst 19. The two correlations are performed using these sets of chips 21a, 21b and the signal generated from the local oscillator 13.

The phasor diagram of Figure 4 shows one potential outcome from performing the two correlations. Two phasors are shown, namely the phasor 23a resulting from the correlation using the first 128 chips 21a of the burst 19, and the phasor 23b resulting from the correlation using the second 128 chips 21b of the burst 19. The phase difference $\Delta\varnothing$ is the difference between these two phasors. The microprocessor 9 is not interested in the (estimated) magnitude of the phase difference but rather the estimated sign of the phase difference, i.e. positive or negative. Here, the estimated sign of the phase difference is positive, and so the frequency difference will also be positive.

Having obtained the estimate of the sign of the phase (and so frequency) difference, the microprocessor 9 then carries out the steps of an algorithm in an attempt to improve (reduce) the phase or frequency difference. The steps of the algorithm are shown in Figure 5.

In an initial step 25 (which is performed prior to the correlation stage described above) the microprocessor 9 stores a so-called frequency modifier (Fmod) variable which is the predetermined amount by which the local oscillator frequency will be initially altered in an attempt to correct the phase/frequency difference. Given that the maximum difference value for this local oscillator is +/- 6 kHz, the initial value of Fmod is set to 6 kHz. An index known as SignOld is also set. This index indicates the previous sign of the phase/frequency difference, although in the initial set-up it is "+". The alteration of the local oscillator 13 using Fmod will be in the negative direction (i.e. its frequency will be reduced) if Fmod is a positive value, and will be in the positive direction (i.e. its frequency will be increased) if Fmod is a negative value.

Step 27 is the correlation step described previously in which the estimated sign of the phase/frequency difference is obtained. This sign is known as SignNew.

In step 29 a comparison is made to determine whether SignNew is "not equal to" SignOld. If the signs are the same, then the local oscillator 13 is modified by an amount equal to Fmod in step 31. Subsequent to this, the procedure is finished if a predetermined amount of time has elapsed. This time is user definable and ultimately depends on the amount of error reduction required. Otherwise, the algorithm returns to step 27 where new correlations are obtained.

In the case where SignNew is not the same as SignOld, the sign of Fmod is changed in step 35. Thus, if Fmod was previously 6 kHz, it will become - 6 kHz in step 35. In step 37, it is determined whether the value of Fmod is less than a value Fmin which is a lower limit set for frequency modification. If Fmod is above this level, then in step 39, the value of Fmod is halved. Accordingly, the -6 kHz will become -3 kHz. The algorithm then returns to step 31 whereby the local oscillator 13 is modified by

increasing its frequency by 3 kHz. The process then repeats. In the case where Fmod is less than Fmin, the value of Fmod will not be halved (since the lower limit is reached) but will remain the same.

It should be appreciated that the principle behind this algorithm is to correct repetitively the phase/frequency difference (using the sign only) such that it will converge around the zero error mark. If, between consecutive paired phase estimates determined in the correlation step 27, the sign of the estimate changes, then the correction made to the local oscillator must have been too large (the zero point having been crossed). The ideal correction will be somewhere between the old local oscillator frequency and the new local oscillator frequency. A form of binary search is employed to try to find the zero crossing between a positive estimate and a negative estimate. Where the estimate tends towards zero, so does the frequency difference.

The above principle is demonstrated with respect to Figure 6, which shows a chart of frequency difference against time. It should be remembered that the microprocessor 9 is not aware of the actual frequency difference shown on the axis, but only the estimated sign of the frequency difference (which can, of course, be derived from the phase difference shown in Figure 4).

The following explanation assumes the initial conditions shown in the flow diagram of Figure 5, and that the frequency difference is actually 4 kHz. The correlation operation will provide a paired phase estimate to get SignNew, which will be positive. In step 29, the comparison will determine that SignNew equals SignOld and so the local oscillator 13 will be modified by reducing the frequency by 6 kHz, taking the actual frequency difference to -2 kHz (this being unknown to the microprocessor 13). After the next correlation, SignNew will be negative (the zero crossing mark having been crossed) and will not be the same as SignOld. Accordingly, Fmod = 6 kHz will become Fmod = - 6 kHz in step 35. This value will be above the value of Fmin (set to about 200 Hz) and so in step 39, Fmod will become - 3 kHz. This will result in the frequency difference becoming 1 kHz.

The above sequence will repeat using the same steps as shown in Figure 5. Accordingly, the next correlation operation will provide a positive difference and so Fmod will become 1.5 kHz. The trend is clearly shown in Figure 6. The result is that the local oscillator frequency will converge about the zero crossing with time being spent in both the positive and negative frequency difference regions. Indeed, it is preferable that roughly equal time is spent with a positive frequency difference as with a negative frequency difference. This is because timing drift occurs when too much time is spent with either a positive or negative frequency difference. If timing drift occurs, reacquisition may be necessary. The above algorithm intrinsically helps to compensate for this problem by spending time in each region (positive and negative frequency errors). This helps to minimise the effect of timing drift.

In the above embodiment, the algorithm is used to provide an initial (coarse) synchronisation in the acquisition stage. Subsequent to this, it becomes possible to access the CPICH on which a known sequence is transmitted. As will be understood by those skilled in the art, the CPICH enables a more fine-tuned synchronisation to be achieved, which is desirable for such a UMTS application. Nevertheless, without the initial, coarse, synchronisation, this would not be possible.

In the above embodiment, reference to a sign change means the sign changes from positive to negative, or vice-versa. However, in the rare event that the sign changes from positive to zero, or negative to zero (so that zero difference is attained) this will constitute a detectable sign change.

The above method and apparatus provides a robust way of improving the frequency difference between a clock signal from a base station and a receiver apparatus having a local oscillator. The convergence to an acceptably small frequency difference is provided quickly, and the algorithm intrinsically compensates for timing drift.

Claims

1. A method of reducing the frequency difference between a local oscillator of a mobile communications receiver and a clock of a remote base station, the method comprising: receiving, at the mobile communications receiver, a synchronisation signal representative of the clock of the base station; performing two consecutive correlation operations on the synchronisation signal to generate an estimate of the sign of the phase difference between the local oscillator and the synchronisation signal; and modifying the local oscillator frequency until the sign of the phase difference changes.

2. A method according to claim 1, wherein the step of modifying the local oscillator frequency comprises modifying the frequency by one or more steps of a predetermined amount.

3. A method according to claim 2, wherein, after the sign of the phase error changes, the method further comprises: modifying the local oscillator frequency by one or more steps of a further predetermined amount until the estimated sign of the phase error changes again, the further predetermined amount being less than that of the previous predetermined amount.

4. A method according to claim 3, wherein the local oscillator frequency is repeatedly modified until the further predetermined amount is reduced to reach a minimum predefined level which is indicative of the phase error converging around the zero error mark.

5. A method according to claim 3 or claim 4, wherein the further predetermined amount is equal to approximately one half of the previous predetermined amount.

6. A method according to any of claims 1 to 5, wherein, between each modification step, a further correlation operation is performed to provide an updated estimate of the sign of the phase error.

7. A method according to any preceding claim, wherein the mobile communications receiver is configured to receive the synchronisation signal over a spread spectrum communications channel.

8. A method according to claim 7, wherein the spread spectrum communications channel transmits data using CDMA modulation.

9. A method according to claim 7 or claim 8, wherein the mobile communications receiver is configured for use with UMTS, the synchronisation signal being received by means of the PSCH.

10. A method according to claim 9, the method further comprising: after synchronisation is achieved using the PSCH channel, opening a further communications channel to provide a further source of synchronisation.

11. A mobile communications receiver for receiving data from a remote base station, the communications receiver comprising: a local oscillator; and a local oscillator controller, the local oscillator controller being arranged to receive a synchronisation signal representative of the clock of the remote base station, to perform two consecutive correlation operations on the synchronisation signal to generate an estimate of the sign of the phase difference between the local oscillator and the synchronisation signal, and to modify the local oscillator frequency until the sign of the phase difference changes.

12. A mobile communications receiver according to claim 11, wherein the local oscillator controller modifies the frequency of the local oscillator by one or more steps of a predetermined amount.

13. A mobile communications receiver according to claim 12, wherein the local oscillator controller is further arranged to modify the local oscillator frequency by one or more steps of a further predetermined amount until the sign of the phase error

changes again, the further predetermined amount being less than that of the previous predetermined amount.

14. A mobile communications receiver according to claim 13, wherein the local oscillator controller is arranged to repeatedly modify the local oscillator frequency until the further predetermined amount is reduced to reach a minimum predefined level which is indicative of the phase error converging around the zero error mark.

15. A mobile communications receiver according to claim 13 or claim 14, wherein the further predetermined amount is equal to approximately one half of the previous predetermined amount.

16. A mobile communications receiver according to any of claims 11 to 15, wherein between each modification step, the local oscillator controller is arranged to perform a further correlation operation to provide an updated estimate of the sign of the phase error.

17. A mobile communications receiver according to any of claims 11 to 16, the receiver being configured to receive the synchronisation signal over a spread spectrum communications channel.

18. A mobile communications receiver according to claim 16, wherein the receiver is configured to receive data which is coded using CDMA modulation.

19. A mobile communications receiver according to claim 11 or claim 18, wherein the mobile communications receiver is configured for use with UMTS, the synchronisation signal being received by means of the PSCH thereof.

20. A mobile communications receiver according to any of claims 11 to 19, the receiver being in the form of a mobile telephone.

21. A method of synchronising a local oscillator of a mobile communications receiver with a clock of a remote base station, substantially as hereinbefore described in the accompanying drawings.

22. A mobile communications receiver for receiving data from a remote base station, constructed and arranged substantially as hereinbefore shown and described in the accompanying drawings.

Application No: GB 0115771.8 15 Examiner: Robert Shorthouse
Claims searched: 1-22 Date of search: 25 February 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H4L (LRPTC, LRPTK, LDSS, LDXX, LDCC, LECF)

Int Cl (Ed.7): H04B 7/26

Other: Online: WPI, EPODOC, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	JP 2000332678	(KOKUSAI) See English language abstract	-
A	JP 070312549	(TOSHIBA) See English language abstract	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier than, the filing date of this application.
&	Member of the same patent family		